#4/Election
OK ON
3/3/03

DOCKET: BUR920010086US1 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor: Bryant et al. Date: February 20, 2003

Serial No.: 09/683,486 Examiner: Samuel A. Gebremariam

Filing Date: 01/07/02 Art Unit: 2811

Title: FIN-BASED DOUBLE POLY DYNAMIC THRESHOLD CMOS FET WITH SPACER GATE AND METHOD OF FABRICATION

FAX RECEIVED
FEB 21 2003
TECHNOLOGY CENTER 2800

RESPONSE TO RESTRICTION REQUIREMENT

Assistant Commissioner of Patents
Washington, DC 20231

Dear Sir:

Responsive to the Office Action mailed January 28, 2003, and the restriction requirement made therein, Applicants provisionally elect, without traverse, the subject matter of Group II, claims 12-25, for continued examination herein. This election is made without prejudice, and with the understanding that Applicants reserve the right to file further applications based on the unelected claims.

Respectfully submitted,

Mark F. Chadurjian
Registration No. 30,739

International Business Machines Corporation
Intellectual Property Law - Mail 972E
1000 River Street
Essex Junction, VT 05452

CERTIFICATE OF FASCIMILE

I hereby certify that, on the date shown below, this correspondence is being faxed to the USPTO addressed to: Assistant Commissioner of Patents, Washington, DC 20231
Attn: Samuel A. Gebremariam, Fax No. 703-872-9318

Date: February 21, 2003 Name: Pat Blair

Signature: Pat Blair